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terminal equipm.
processing needs

vector processing
or DSP task

scalar processing
or non-DSP task

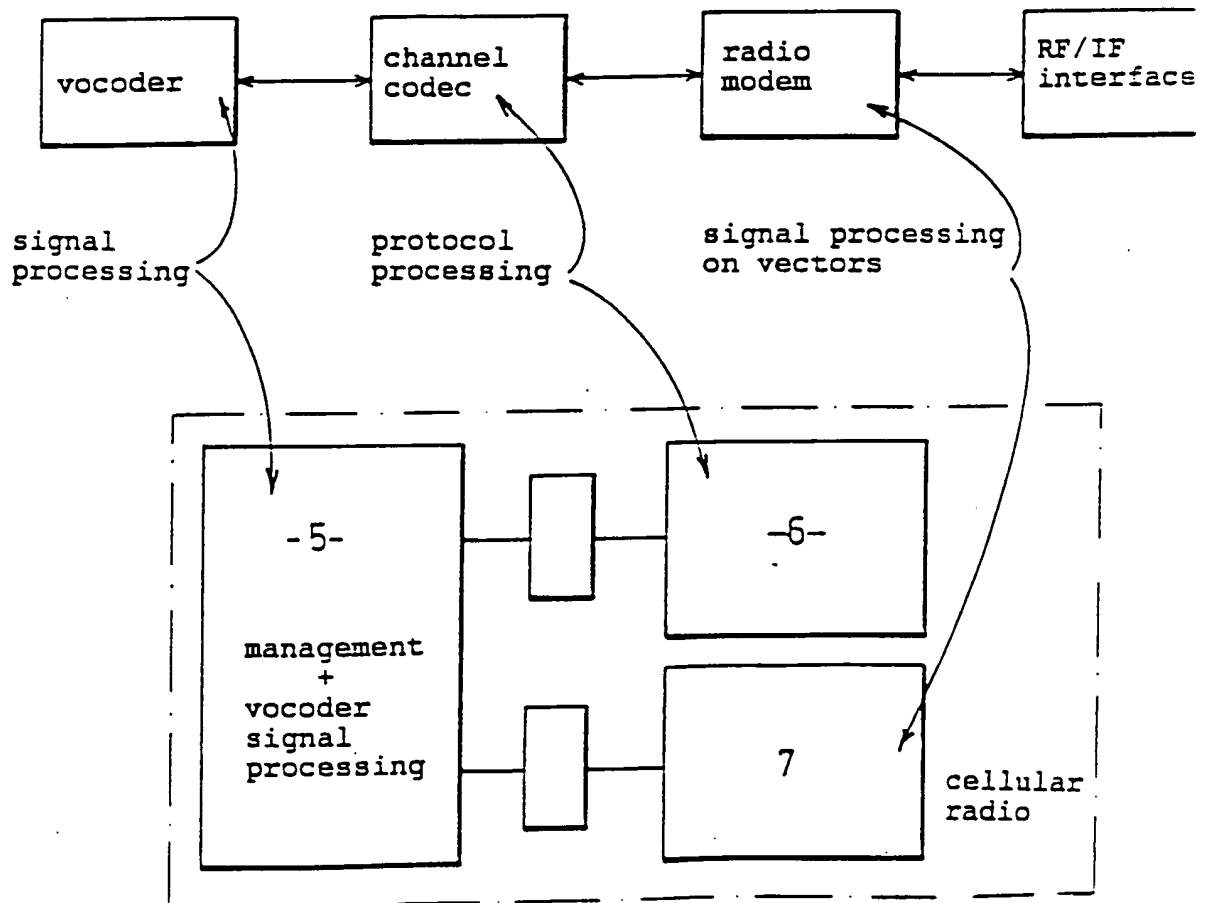
-4-

2

1

-3-

FIG. 1



PERFORMANCE OF CHANNEL CODEC ROUTINES

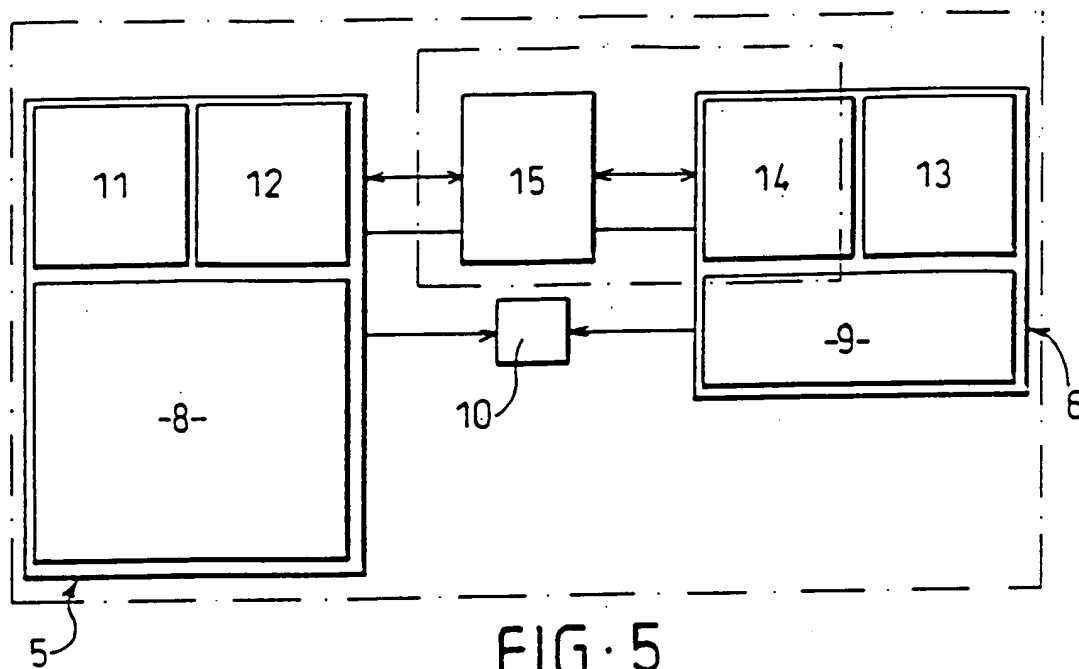
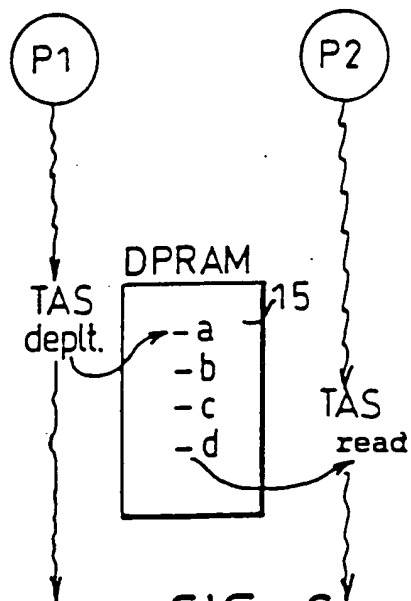
routines	DSP utilisation C5x	proc. protocol PP utilisation
16 bit CRC identification	6 instr/ bit 5 instr/ bit	4 instr/ bit 1 instr/ bit
RATIO		
sel/instr efficiency no. of trans. MIPS	$\times 1$ 58 KTx 28 MIPS	$\times 2.2$ 6.5 KTx $28 \times 2.2 = 62$ MIPS DSP

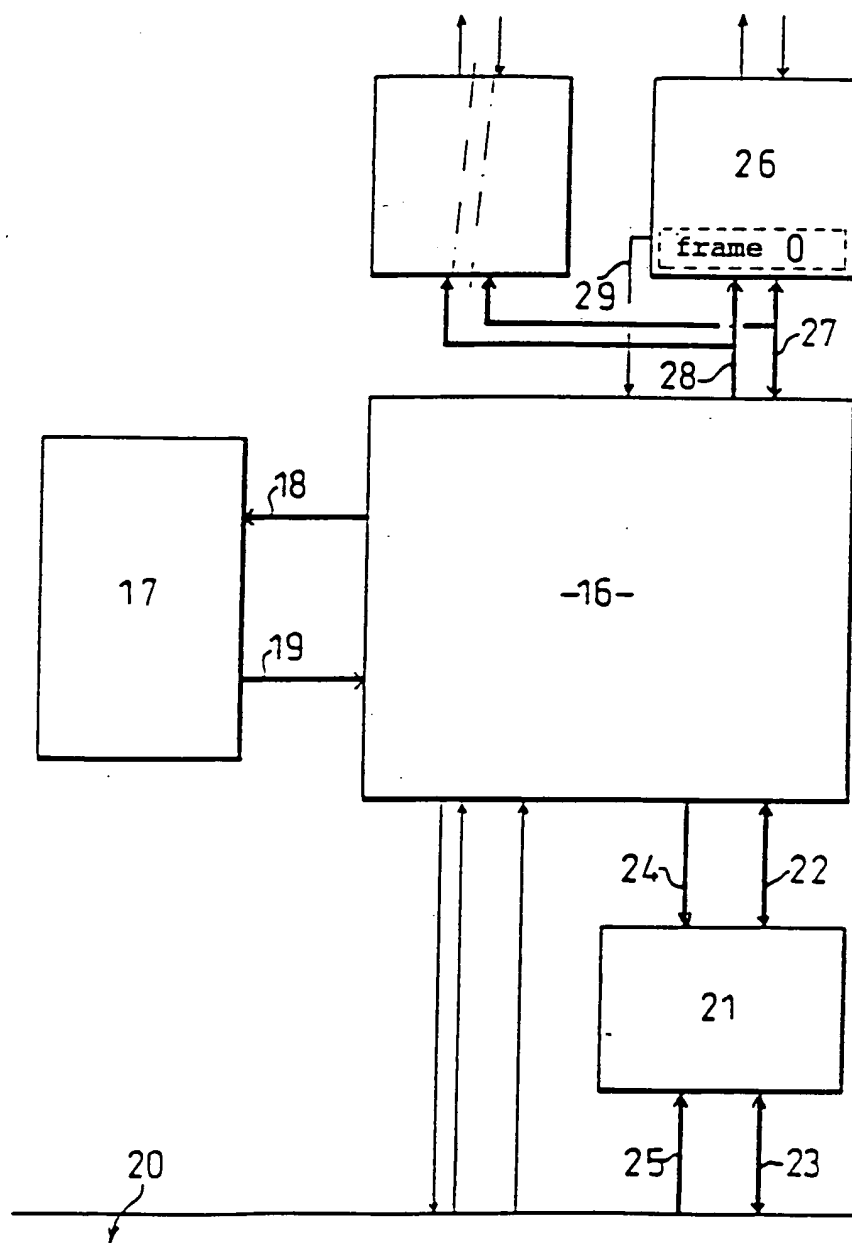
FIG. 3

PERFORMANCE OF MODEM ROUTINES

routines	DSP utilisation C5x	array proc.
metric computation 57 symbols (4 samples)	43800 cycles	4400 cycles
RATIO		
instruction setting efficiency MIPS	$\times 1$ 28 MIPS	$\times 10$ $28 \times 10 = 280$ MIPS DSP

FIG. 4

FIG. 5FIG. 6

FIG. 7

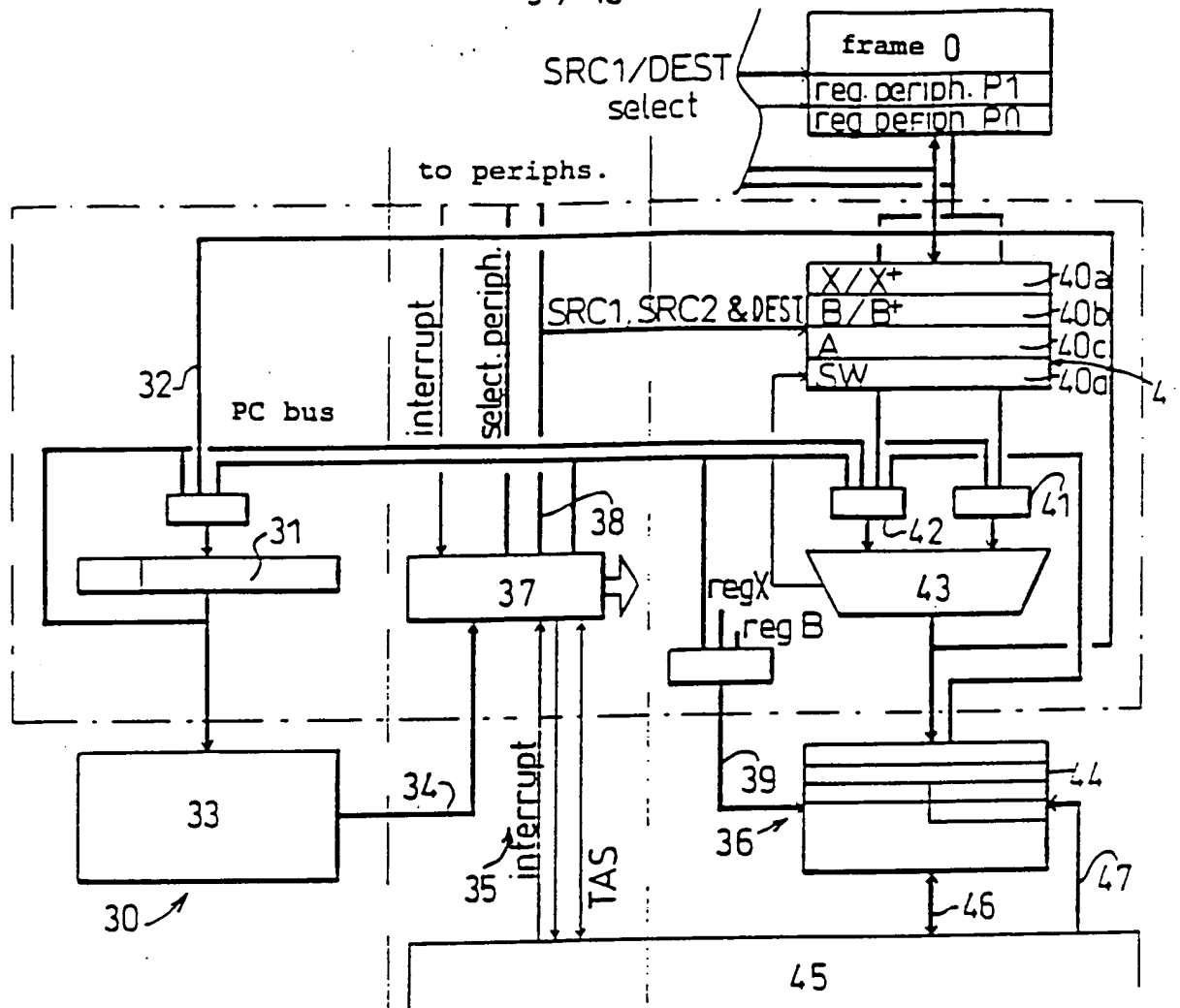


FIG. 8

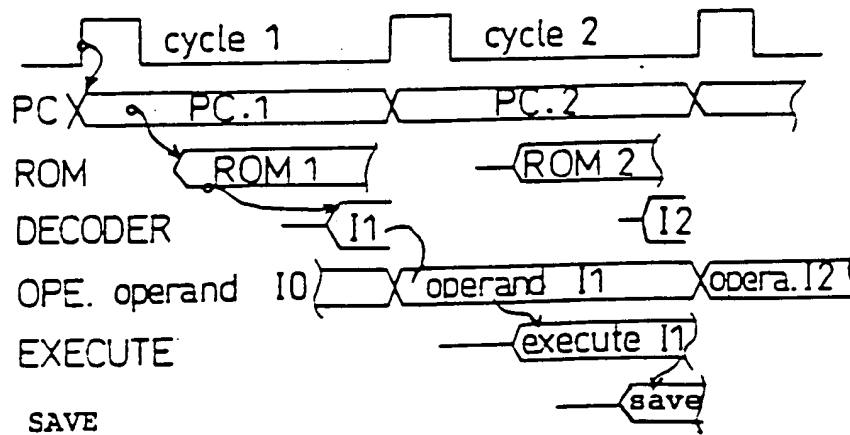


FIG. 9

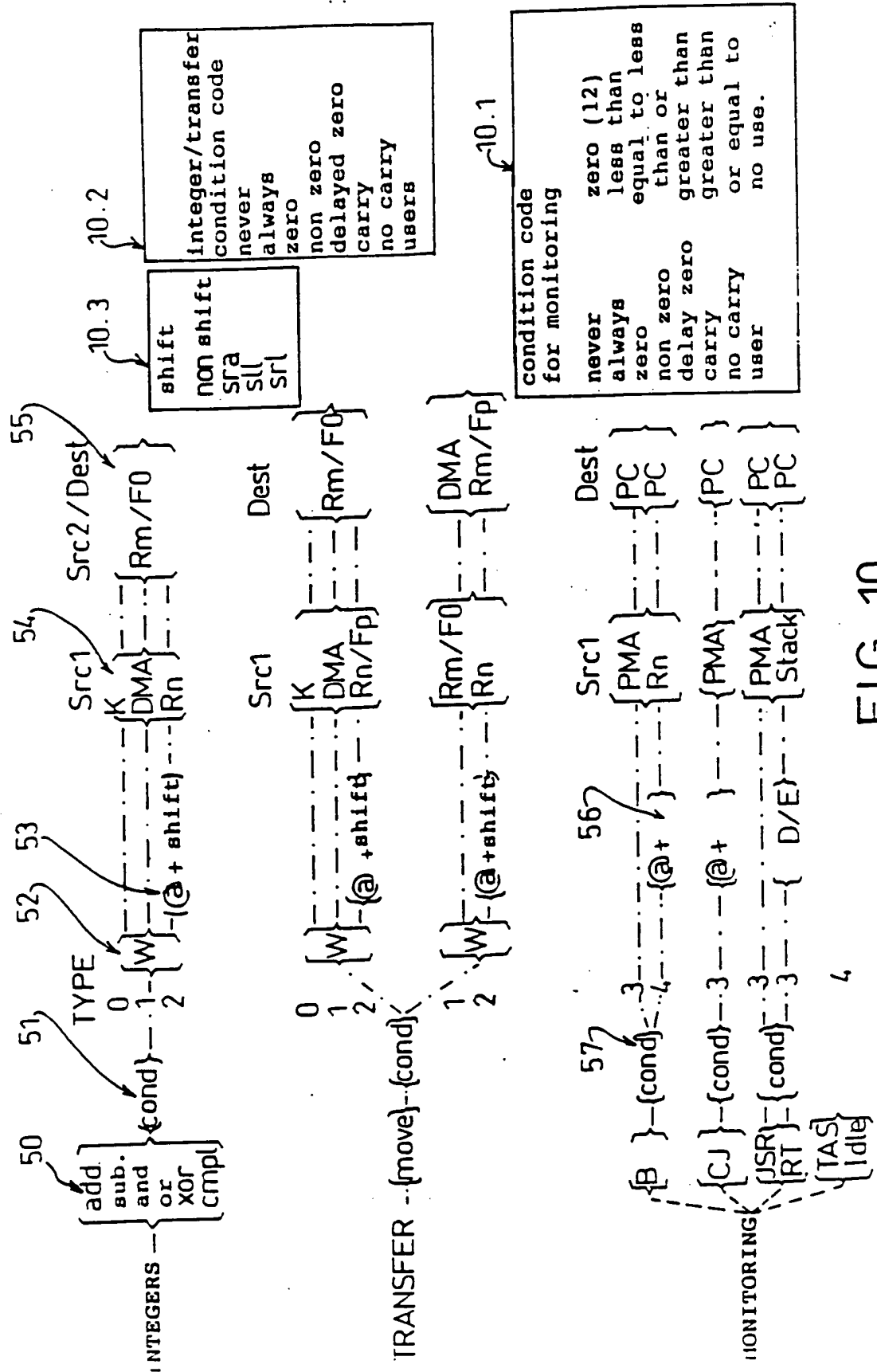


FIG. 10

op code											
TYPE											
0	0_0	ALU	Cc	1	K	WI	Rm		K		integer/ transfer
1	0_1	ALU	Cc	1	DMA	WI	Rm		DMA	IL	
2	1_0	ALU	Cc	1	@	WI	Rm	Rn	FP	S	
3	1_1	code	Cc		@	DWI			PMA		monitor
4	1_1	code	Cc		@	WI		Rn			

FIG. 11

ALU		Code		Cc	
0	- sub	0	- ST type 1	0	- never
1	- CPL	1	- ST type 2	1	- always
2	- add	2	- B type 3	2	- Z
3	- and	3	- B type 4	3	- NZ
4	- or	4	- CALL	4	- ZD
5	- XOR	5	- RTS	5	- C
6	- PASSA	6	- RTI	6	- NC
7	- SUBC	7	- STOP	7	- user

Rm/Rn		W		L		S	
0	- PO	0	- R/W byte	0	- Rm low	0	- PASS
1	- P1	1	- R/W word	1	- Rm high	1	- SRA
2	- A					2	- SLL
3	- B					3	- SRL
4	- X						
5	- PC						
6	- SW						
7	- SP						

L	
0	- DMA/Rn low
1	- DMA/Rn high

FIG. 12

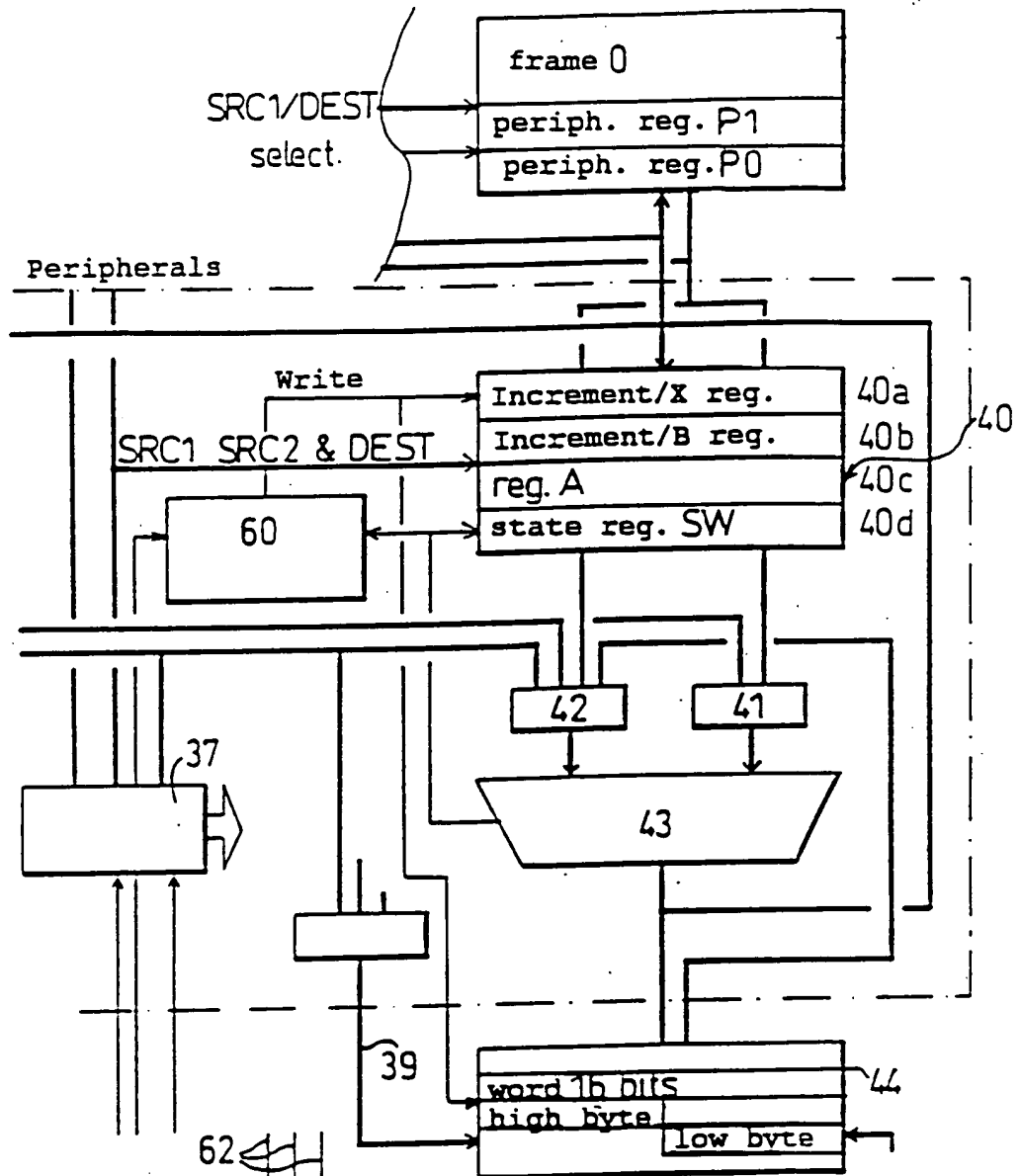


FIG. 13

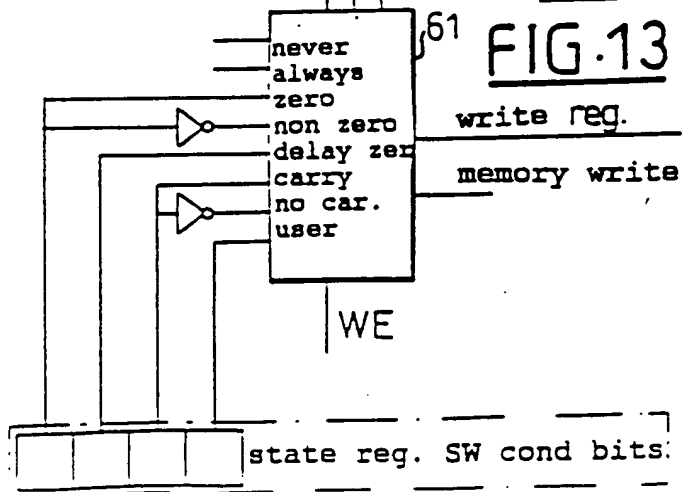


FIG. 14

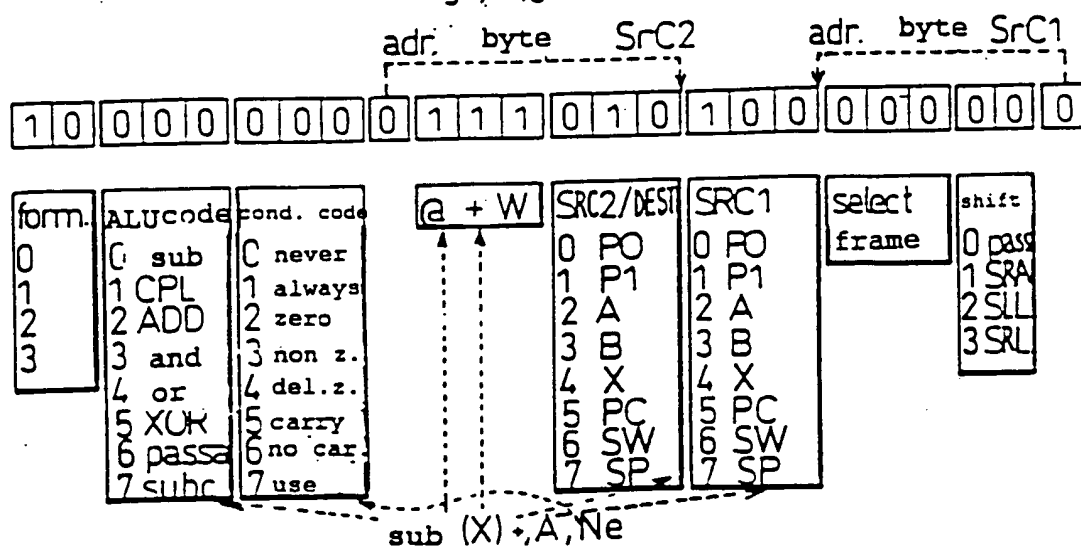
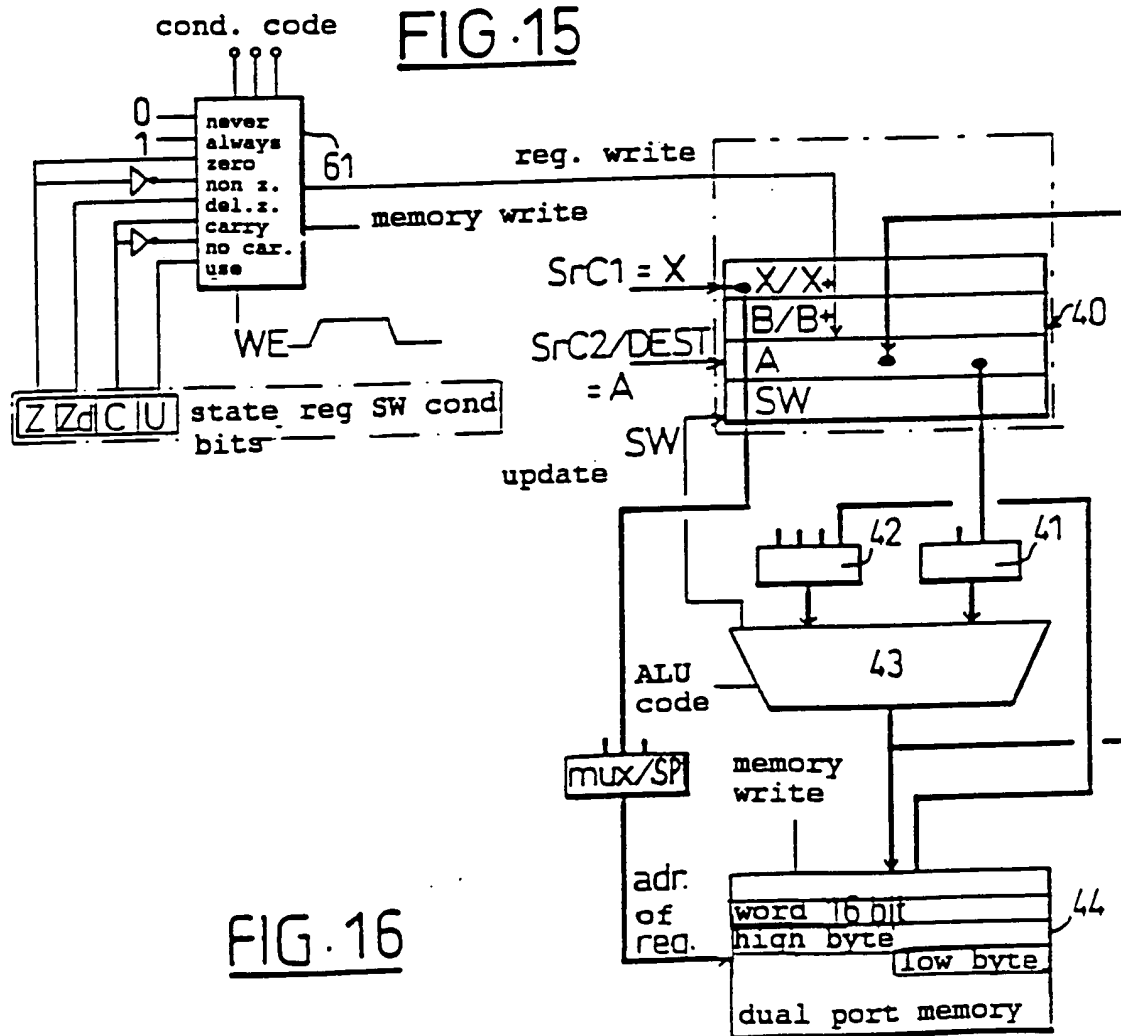
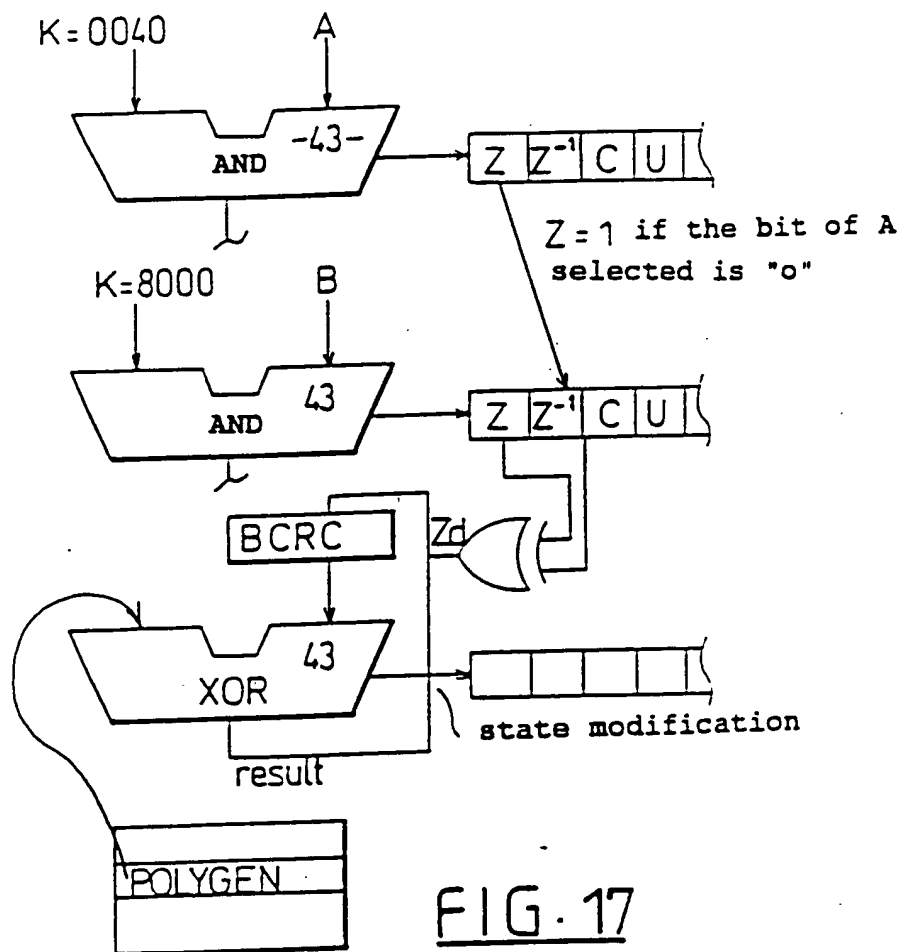


FIG. 15



FIG. 17